10. The source driver of claim **8**, wherein the first node is provided between the second transistor and the bias device, and the second node is provided between the fourth transistor and the bias device.

11. The source driver of claim **8**, wherein the first node is provided between the first transistor and the second transistor or between the second transistor and the bias device, and

the second node is provided between the third transistor and the fourth transistor or between the fourth transistor and the bias device.

12. A source driver comprising:

a plurality of buffers, each of the buffers respectively comprising an amplifier configured to amplify an input signal and an output driver configured to output a driving signal to a data line,

wherein the amplifier comprises a bias device configured to receive a bias voltage and a first current mirror connected between a first voltage and the bias device, and

the first current mirror comprises:

a first transistor and a second transistor forming a first reference current path and connected in series to each other between the first voltage and the bias device,

a third transistor and a fourth transistor forming a first output current path and connected in series to each other between the first voltage and the bias device, and

a first switch electrically connecting the first reference current path to the first output current path.

13. The source driver of claim **12**, wherein the first reference current path comprises:

a first node provided between the first transistor and the second transistor, and

a second node provided between the second transistor and the bias device, and

the first output current path comprises a third node provided between the third transistor and the fourth transistor and a fourth node provided between the fourth transistor and the bias device.

14. The source driver of claim **13**, wherein the switch comprises a first electrode connected to the first node or the second node, and further comprises a second electrode connected to the third node or the fourth node.

15. The source driver of claim **13**, wherein the first current mirror further comprises a second switch electrically connecting the first reference current path to the first output current path,

the first switch is connected between one of the first node and the second node and one of the third node and the fourth node, and

the second switch is connected between the other of the first node and the second node and the other of the third node and the fourth node.

16. The source driver of claim **12**, wherein the amplifier further comprises a second current mirror connected between a second voltage and the bias device, and

the second current mirror comprises:

a fifth transistor and a sixth transistor forming a second reference current path and connected in series to each other between the second voltage and the bias device,

a seventh transistor and an eighth transistor forming a second output current path and connected in series to each other between the second voltage and the bias device, and

a second switch electrically connecting the second reference current path to the second output current path.

17. The source driver of claim **16**, wherein the first voltage is a power voltage and the second voltage is a ground voltage.

18. The source driver of claim **16**, wherein the second reference current path comprises a fifth node provided between the fifth transistor and the sixth transistor and a sixth node provided between the sixth transistor and the bias device, and

the second output current path comprises a seventh node provided between the seventh transistor and the eighth transistor and an eighth node provided between the eighth transistor and the bias device.

19. The source driver of claim **18**, wherein the output driver comprises:

a first driving transistor comprising a gate connected to the fourth node,

a second driving transistor comprising a gate connected to the eighth node,

a first compensation capacitor comprising an electrode connected to the third node;

a second compensation capacitor comprising an electrode connected to the seventh node,

a first enable switch connected between the fourth node and the gate of the first driving transistor, and

a second enable switch connected between the eighth node and the gate of the second driving transistor.

20. An output buffer of a source driver having a feedback path, the output buffer comprising:

an inputter configured to receive a gradation voltage and a feedback voltage as input signals;

an amplifier configured to perform an amplification operation based on the input signals and thereby generate an output signal, the amplifier comprising a first current mirror connected to a first voltage, a second current mirror connected to a second voltage, and a bias device connected between the first current mirror and the second current mirror, the first current mirror comprising at least two nodes provided inside the first current mirror; and

an output driver configured to generate a driving signal for driving a data line, based on an output signal of the amplifier,

wherein the first current mirror comprises a first switch configured to electrically connect the at least two nodes provided inside the first current mirror to each other during a charge sharing operation.

21-28. (canceled)

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